REMARKS

Attached hereto is a marked up version of the changes made in the specification and claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**"

It is noted that the claim amendments herein are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-19 are all of the claims pending in the present Application. Claims 1-6 and 14-18 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,201,383 to Lo et al, further in view of US Patent 5,103,557 to Leedy. Claim 7 stands rejected under 35 USC §103(a) as unpatentable over Lo et al, further in view of US Patent 5,420,500 to Kerschner. Claim 8 stands rejected under 35 USC §103(a) as unpatentable over Lo et al, further in view of US Patent 5,438,272 to Craig et al. Claims 9-13 and 19 stand rejected under 35 USC §103(a) as unpatentable over Lo et al, further in view of Leedy, and further in view of Kerschner. These rejections are respectfully traversed in view of the following discussion.

I. THE CLAIMED INVENTION

As described and claimed, e.g., by claim 1, the present invention is directed to an electronic circuit test and repair apparatus including at least one wiring analyzer to locate shorts between conductors on a surface of or embedded in a carrier substrate. The conductors are intended to interconnect components *to be mounted* on the carrier substrate to form a circuit. A current source provides current sufficient to remove the shorts. At least two probes contact the conductors in a manner controlled by the wiring analyzer.

II. THE PRIOR ART REJECTION

The Examiner asserts that US Patent 6,201,383 to Lo et al., further in view of US Patent 6,288,561 to Leedy, renders obvious the present invention as described by claims 1-6 and 14-18.

The Examiner concedes that Lo fails to teach or suggest an apparatus capable of providing current to remove shorts. To overcome this deficiency, the Leedy reference is introduced. The Examiner asserts that "it would have been obvious to one skilled in the art at the time of the invention to use the current source of Leedy in the apparatus of Lo et al. for the additional purpose of removing shorts and repairing electronic circuits since it is stated by Lo et al. that "it is desirable to determine which networks are shorted together, so that the circuit can be repaired" (column 6, lines 54-56)."

Applicants respectfully traverse that this combination is appropriate since, to one of ordinary skill in the art, the Leedy reference addresses an entirely different type of test apparatus and test purpose, and there is no suggestion in Leedy to apply the techniques described therein into the technology of the present invention test apparatus.

More specifically, the test set in Leedy is a burn-in/repair apparatus to be used in the semiconductor technology, in which a wafer having integrated circuits is tested. These integrated circuits inherently include a number of active semiconductor devices to form an active circuit already completed on the substrate.

In contrast, the present invention addresses the technology of printed circuit boards/ substrates in which *no components have yet been mounted*. The conductors of the boards/substrates of the present invention are ranges of magnitude larger in dimension than those used in the technology addressed by the Leedy reference. The apparatus described in Leedy would not have sufficient energy to repair the short circuit defects on printed circuit boards. As described on page 8 of the instant disclosure, the current levels of the present invention is measured in amperes rather than microamperes or milliamperes of the Leedy apparatus and the voltage level can be as high as 100 volts.

In fact, the primary reference Lo represents perfectly the problem addressed by the present invention. That is, at page 2 of the disclosure of the instant Application, it is described how the printed circuit board/substrate technology is conventionally confined to the technique in which these short circuits are removed by a very time-consuming manual technique. Neither Lo nor Leedy make any suggestion to use the solid state technique of Leedy in the apparatus described by Lo. The rejection on record merely takes advantage of hindsight and is clearly prohibited as meeting the burden of a *prima facie* rejection under 35 USC §103(a).

None of the other references cited by the Examiner overcomes this basic deficiency. That is, none provides a suggestion to combine a high current source required to remove short circuits on a printed circuit board into an apparatus having a function of locating these short circuits on a board or substrate that is yet unpopulated by components. Advantages of providing an automated short circuit removal technique into the apparatus used to test for and isolate the short circuits include considerable savings in time and cost and considerable savings in scrapped materials.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of " ... at least one wiring analyzer to locate shorts between conductors on a surface of a carrier substrate, said conductors intended to interconnect components to be mounted on said carrier substrate to form a circuit; a current source to provide current sufficient to remove said shorts...," as clearly required by claim 1. Independent claims 9, 11, 14, and 19 have corresponding terminology "interconnect packages".

For this reason alone, the claimed invention is fully patentable over the cited references.

Additionally, Applicants respectfully traverse the Examiner's contention that simply combining the Leedy reference with the Lo reference provides a justification that a second analyzer is thereby rendered obvious. That is, neither reference provides even a hint of using a second analyzer. The advantage provided by the optional second analyzer of the present invention is unique to the specific environment of the packaging technology in which a relatively high current is required to repair the short circuits. Relay switching is better suited for these higher currents but is considerably slower compared to solid state switching. The

present invention optionally incorporates the second analyzer to provide a faster testing time, reverting to the relay switching to do the repair attempts once a short circuit has been found.

None of the references cited by the Examiner make any suggestion for a second analyzer. As MPEP §2143.01 points out, "[t]he mere fact that references can be combined or modified does not render the resultant invention obvious unless the prior art also suggests the desirability of the combination" (emphasis in MPEP).

Additionally, relative to the rejection for claims 5 and 17, Applicants respectfully assert that none of the references cited by the Examiner make any suggestion for the high voltage stress test incorporated as an automatic feature of the present invention. This test is much more than the vague suggestion that the Examiner points to of "high voltage or current" at lines 60-64 of column 6 of the Leedy reference "to open up a conducting path". The high voltage stress test of the present invention, as described at lines 10-13 of page 12, is actually addressing the problem of re-growth of the just-removed short circuit. As indicated at lines 7-12 of page 13, this voltage stress test will have parameters that are adjusted based on materials used for the conductors and dielectric. The Leedy reference does not reasonably provide any suggestion for such high voltage stress testing nor even discusses this problem.

For the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with the Lo, Leedy, Kerschner, or Craig, fails to teach or suggest the claimed invention.

IV. FORMAL MATTERS AND CONCLUSION

The Examiner objected to Figure 1 as requiring a lead line for numeral 18 and a "Prior Art" label. Applicants submit under separate cover a Submission of Proposed Drawing Changes that is believed to address the Examiner's concern.

The Examiner also objected to the specification at line 3 on page 9 and at line 19 on page 12 because the verb "is" is considered as requiring to be replaced by the verb "are". Applicants respectfully decline to make this change at this time since it is considered to be in correct English as written. That is, the subject of the sentence at line 3 on page 9 is

"plurality", and the subject of the sentence at line 19 on page 12 is "none". In both cases, the subject is singular and requires the singular verb form "is" rather than the plural form "are".

In view of the foregoing, Applicant submits that claims 1-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview. The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:
The claims have been amended, as follows:

1. (Amended) An electronic circuit test and repair apparatus, comprising:

at least one wiring analyzer to locate [circuit] shorts between conductors, said conductors being on a surface of or embedded in a carrier substrate, said conductors being intended to interconnect components to be mounted on said carrier substrate to form a circuit;

a current source to provide current sufficient to remove said shorts; and

at least two probes to contact [a circuit under evaluation] said conductors in a manner controlled by said wiring analyzer.